

Appl. No. 10/698,130  
Amdt. dated December 14, 2004  
Reply to Office action of September 23, 2004

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A computer system, comprising:  
an interconnect;  
a plurality of processor nodes, coupled to the interconnect, each processor node comprising[[;]] at least one processor core, each processor core having an associated memory cache for caching memory lines of information;  
a plurality of input/output nodes coupled to the interconnect; and  
wherein the processor nodes and the input/output nodes collectively comprise a plurality of system nodes, each of which comprises[[;]]  
  
Input logic for receiving that receives a first invalidation request, the invalidation request identifying a memory line of information and including a pattern of bits for identifying that Identify a subset of the plurality of system nodes that potentially store cached copies of the identified memory line; and  
  
processing circuitry that, responsive to receipt of the first invalidation request, for determining determines a next node identified by the pattern of bits in the invalidation request and for sending sends to the next node, if any, a second invalidation request corresponding to the first invalidation request, and for invalidating that invalidates a cached copy of the identified memory line, if any, in the particular node of the computer system.

2.-8. (Canceled).

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9. (Currently amended) A computer system, comprising:

- a plurality of multiprocessor nodes, each multiprocessor node comprising[[;]]
  - a multiplicity of processor cores, each processor core having an associated memory cache for caching memory lines of information;
  - a plurality of input/output nodes coupled to the plurality of multiprocessor nodes; and
- wherein the multiprocessor nodes and the input/output nodes collectively comprise a plurality of system nodes, each of which comprises[[;]]
  - input logic for receiving that receives a first invalidation request, the invalidation request identifying a memory line of information and including a pattern of bits for identifying a subset of the plurality of system nodes that potentially store cached copies of the identified memory line; and
  - processing circuitry that, responsive to receipt of the first invalidation request, for determining determines a next node identified by the pattern of bits in the invalidation request and for sending to the next node, if any, a second invalidation request corresponding to the first invalidation request, and for invalidating that invalidates a cached copy of the identified memory line, if any, in the particular node of the computer system.

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10.-16. (Canceled).

17. (Previously presented) The system of claim 1 wherein the system is reconfigurable so as to include any ratio of processor nodes to input/output nodes so long as a total number of processor nodes and input/output nodes does not exceed a predefined maximum number of nodes.

18. (Previously presented) The system of claim 1 wherein each processor node and input/output node further comprises a protocol engine implementing a predefined cache coherency protocol, wherein the protocol engine of each processor node is functionally identical to the protocol engine of each input/output node.

19. (Previously presented) The system of claim 9 wherein the system is reconfigurable so as to include any ratio of multiprocessor nodes to input/output nodes so long as a total number of multiprocessor nodes and input/output nodes does not exceed a predefined maximum number of nodes.

20. (Previously presented) The system of claim 9 wherein each multiprocessor node and input/output node further comprises a protocol engine implementing a predefined cache coherency protocol, wherein the protocol engine of each multiprocessor node is functionally identical to the protocol engine of each input/output node.